program four FPGAs (**Figure 1**).

A DSP processor, the ADSP21065L, serves as a microcontroller to program the FPGAs. The configuration bus consists of the Clk, Data, Program, Init, and Done signals. The output data from the ADSP21065L is synchronous with the Clk signal, and the Program (output), Init (input), Done (input), and two control signals (output) are the ADSP21065L's I/O flags. The rest of the circuit comprises four FPGAs from Xilinx. The arrows to the FPGAs represent the configuration bus. The trick is in the so-called switchboard, which traces the configuration bus to an FPGA according to the ADSP-21065L's control signals. At first thought, some bidirectional buffers, for example, 74LVT16245s, would seem suitable for this requirement by linking the control signals to OE and T/R pins of the buffers.

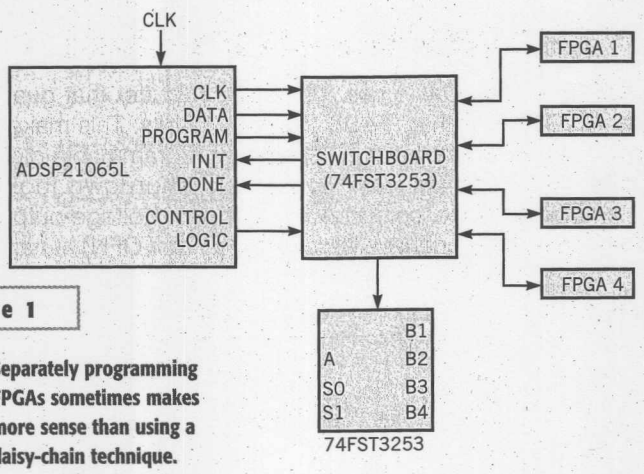

Figure 1 **Separately programming FPGAs sometimes makes more sense than using a daisy-chain technique.**

But after taking a closer look at the situation, this approach would be difficult because the Init and Done are output signals from the FPGAs, which you cannot merge together. Therefore, the "buffer" you are looking for should have multiplexing or demultiplexing capabilities. This design uses the 74FST3253 dual 4-to-1 multiplexer/demultiplexer bus switch from On Semiconductor (www.onsemi.com) to implement this function. By connecting two control signals to the two select inputs, S0 and S1, you can cause I/O Signal A to connect to I/O lines B1, B2, B3, or B4, respectively, if the value of the two control signals are 00, 01, 10, or 11.□

Add fault protection to a 4- to 20-mA loop supply

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A 4- TO 20-mA CURRENT LOOP consists of a power source and a current-measuring device at the control end and a field transmitter that senses process-variable information, such as temperature or pressure, and converts it to a current (**Figure 1**). Most such industrial current loops are powered by 24V dc, but that voltage can range from 12 to 36V. The loop voltage in older systems can be even higher. Many such applications require current limiting, fault protection, or both. For example, a short circuit or another high-current fault in one of several loops powered by a single source can produce a power-supply failure that disables all transmitters powered by that source. Intrinsically safe loops, on the other hand, include a barrier module that limits current and voltage to the transmitter. Fault-protected sources can add another level of system safety. Setting a current limit on each loop lets you accurately size the power supply without overspecifying it. **Figure 2** shows one form of flexible fault protection for the 24V power supply of a 4- to 20-mA loop. It also includes circuitry for recovering a digital signal superimposed on that loop. IC_1, a high-side current-sense amplifier with comparator and reference, senses the loop current in R_1 as an 8- to 40-mV voltage and amplifies it by 100, producing an output-voltage range of 0.8 to 4V. That output, V_{OUT}, can directly drive external meters, strip-chart recorders, and A/D-converter inputs.

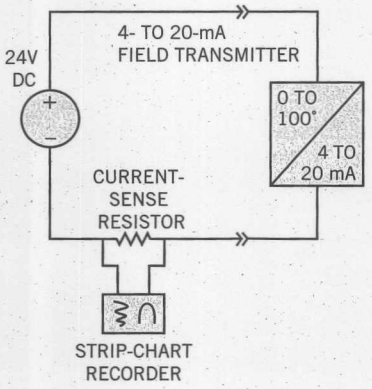

Figure 1 **Industrial applications widely use the basic structure of a 4- to 20-mA current loop.**

The R_2-R_3 voltage divider sets the selected fault-current trip point for IC_1's first internal comparator at 0.6V. Setting the trip point for a 50-mA fault, for instance, establishes the following relationship between R_1 and R_2: $R_2/(R_1+R_2)=0.6V/(R_1\times100\times I_{FAULT})$, so $R_1=15.67\times R_2$. When faults occur, the C_{OUT1} output assumes a high-impedance state and is pulled high by R_3. The noninverting cascaded-transistor pair Q_2-Q_3 provides an interface to the high loop voltage and preserves a proper logic polarity for controlling the gate of Q_1. Q_1 is held in the off state until pushbutton PB_1 or another reset signal resets IC_1's first comparator. (To disable this comparator's latched output, tie the Reset# pin to ground.) Zener diode ZD_1 protects Q_1's gate-source junction from overvoltage.

IC_2 and its associated circuitry can recover any digital information imposed on the 4- to 20-mA loop current by modu-

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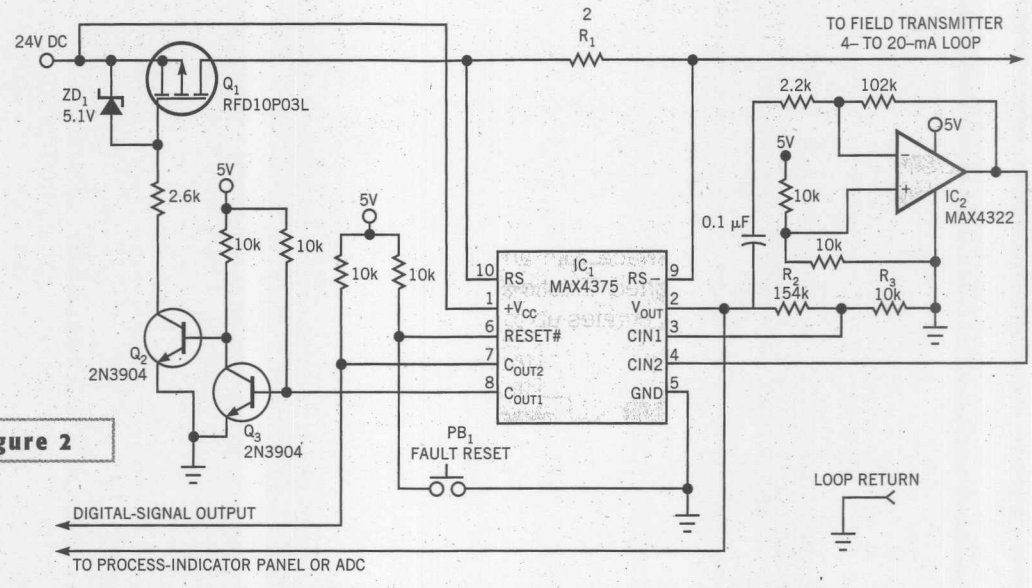

Figure 2 This circuit provides fault protection and digital-signal recovery for a 4- to 20-mA current loop.

lation. The Highway-Addressable Remote Transducer Protocol, for instance, typically uses FSK (frequency-shift keying) of 1200 to 2400 Hz to modulate the loop current between the ±0.5mA levels. (For this circuit, the modulated signal at V_{OUT} (Pin 2 of IC_1) is ±0.1V.) V_{OUT} from IC_1 is capacitively coupled to IC_2 and amplified by that device to recover such digital signals. IC_1 includes a second comparator with inverting input, which you can use to cancel the inversion in IC_2's digital-signal output. Though not essential, this comparator output (C_{OUT2}) can also present the recovered digital signal as a clean rectangular waveform for driving external circuitry.□